HawkEye-CL

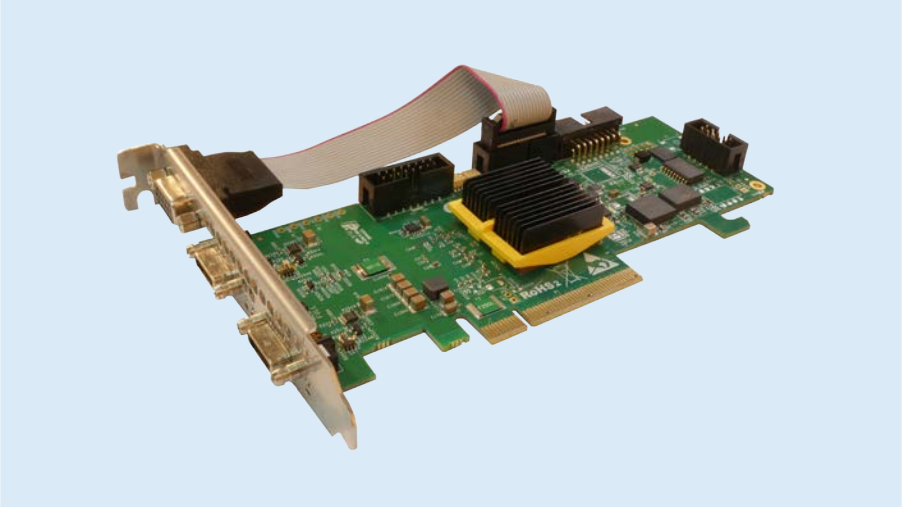
Camera Link Frame Grabbing and Image Processing System

Key Features

- Camera Link Rev. 2.0 compliant
- Camera Link modes: Base, Medium, Full, 80-bit (Deca)
- Option for connecting two Base cameras
- Pixel formats supported: Mono, Bayer, RGBA (8, 10, 12, 14 and 16 bits/color) and RGB (8, 10 and 12 bits/color).
- Huge frame buffers of up to 16 GB to enable high-acquisition capacity and to enhance image processing capabilities.
- Ultra-high data offload capability of up to 64 Gb/s, enabling high-resolution post processing on host computer.
- Infrastructure for full Vision/Imaging system solutions, including image acquisition, real-time image processing, and post-processing on host.
- Flexibility to realize any camera interface and protocol for streaming the camera data directly to the FPGA.
- Powerful tools for efficient development of both software and FPGA code.

Target Application Examples

- Automotive and Inspection applications demanding real-time analysis and system response.
- Military & Aerospace applications combining real-time and post-acquisition analysis.
- Medical & Scientific applications requiring high-resolution imaging capabilities.
- Traffic & Transportation applications processing high-volume data from multiple locations.



The Gidel HawkEye-CL frame grabbing and real-time image processing system provides the core infrastructure required to support the most demanding Vision and Imaging applications.

The HawkEye series offers a number of options to accommodate diverse application needs, from plug-and-play high-performance frame grabbers to a full system solution that comprises acquisition, open-FPGA image processing, and a flexible custom camera interface. Off-the-shelf HawkEye solutions include support for Camera Link and CoaXPress cameras.

The HawkEye-CL is Camera Link Rev. 2.0 compliant and supports 80-bit Camera Link modes, including 10-bits/8-tap and 8-bit/10-tap modes. The HawkEye-CL family is based on PCIe Gen. 3 x8, providing CPU-free ultra-fast offload capacity of up to 64 Gb/s. Huge data buffers of up to 16 GB fortify the acquisition bandwidth and the image processing capabilities on powerful Arria 10 FPGAs.

The HawkEye is supported by Gidel's Proc Developer's kit, which includes the ProcFG GUI application, an API library and examples for developing a customized application, and the ProcWizard application for efficient development of image processing algorithms on FPGA. The HawkEye-CXP is also supported by Gidel's HLS application support package for compiling untimed C++ code to FPGA HDL code using Intel's HLS compiler.

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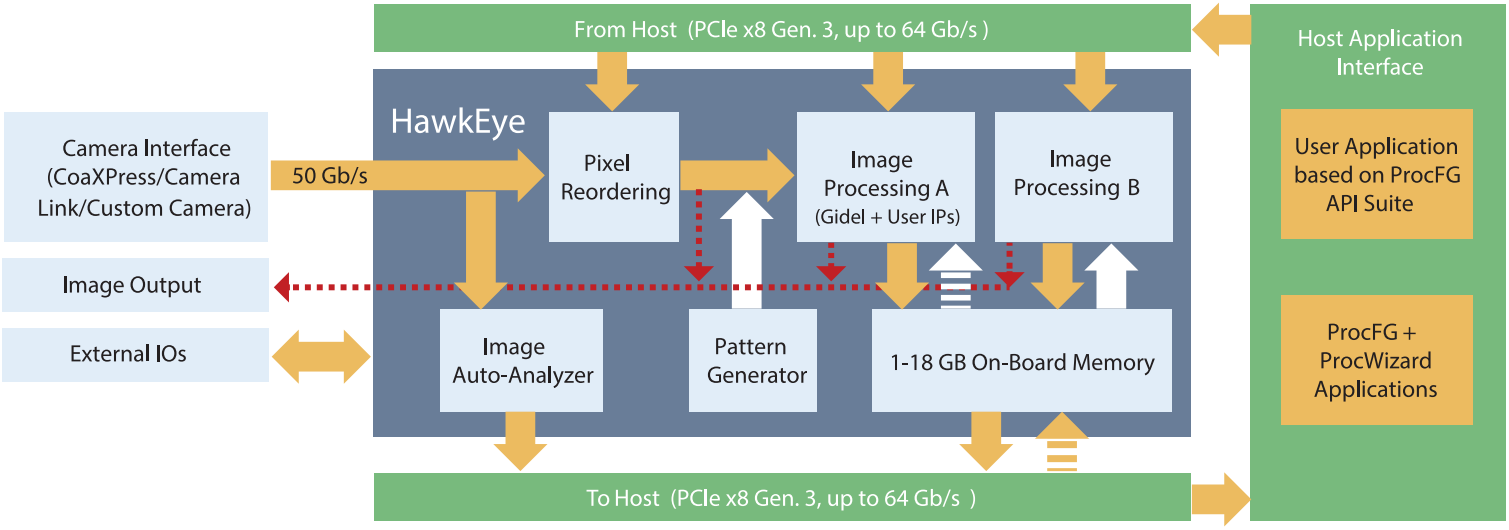
HawkEye-CL Camera Link Acquisition and Image Processing System

FEATURE	SPECIFICATIONS
Camera Interface	1 80-bit (Deca), Full, Medium or Base Camera Link or 2 Base Camera Links with option for PoCL
Image Formats	Mono, Bayer, RGBA (8, 10, 12, 14 and 16 bits/color) and RGB (8, 10 and 12 bits/color).
Max. Resolution	Horizontal: 16 K pixels (64-bit) Vertical: 65 K lines
Tap Configuration	All configurations as defined by the Camera Link standard, including 80-bit (Deca): 10 taps/8bits, 8bits/10taps.
Connectors	2x SDR26 (mini Camera Link) VGA15-pin I/O
Pixel Clock	Up to 85 MHz
Acquisition Rate	Up to 50 Gb/s acquisition rate
Host Bus	PCIe x8 Gen. 3
Host Throughput	Up to 64 Gb/s
Frame Buffer	1-16 GB

FEATURE	SPECIFICATIONS
Form Factor	PCIe low-profile
MTBF	> million hours
Camera Types	Area and Line
GPIO	RS422, opto-coupler, LVTTL and 30V at 0.9A
Advanced Features	Selective ROI acquisition
Software Support	ProcFG GUI, API and examples. For open FPGA grabber version, ProcWizard Development tool
OS Support	Win 7, 10 and Server 2012 (64-bit) and Linux (kernel 2.6.x- 3.10.x). Linux version doesn't include ProcFG GUI
Image Processing	For open FPGA grabber version, option for adding image processing code on Altera Arria 10 FPGA
Certifications	RoHS, Conflict Minerals, ISO
Operating Ambient Temperature	0 – 54 C, relative humidity up to 90% (non-condensing)



Typical HawkEye acquisition and processing system implementation

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HawkEye-CXP

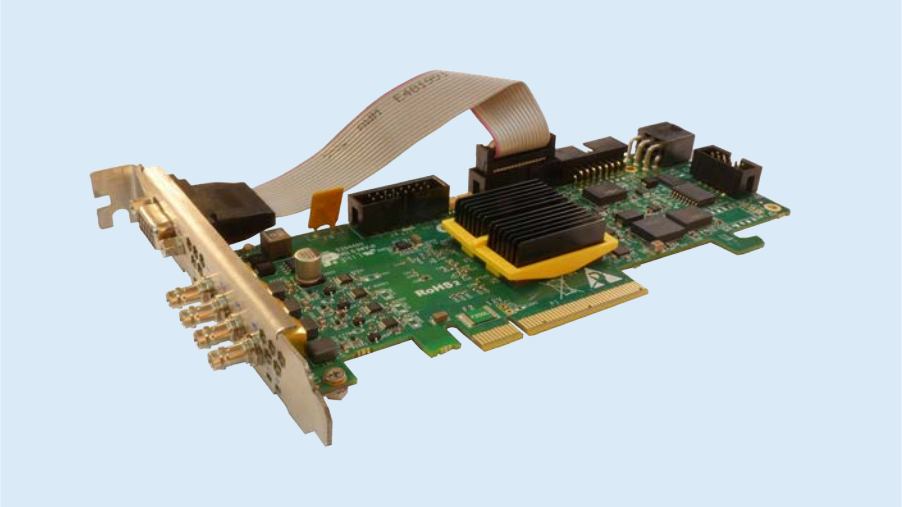
CoaXPress Frame Grabbing and Image Processing System

Key Features

- Grabbing from 1, 2 or 4 cXp cameras via up to 25 Gb/s (4x cXp-6 links)
- Pixel formats supported: Mono, Bayer, RGBA and RGB
- Acquisition bandwidth of up to 25 Gb/s
- Infrastructure for full Vision/Imaging system solution including image acquisition, real-time image processing and post-processing on host
- Huge frame buffers of up to 16 GB to enable high-acquisition capacity and to enhance image processing capabilities
- Ultra-high CPU-free data offload capability of up to 64 Gb/s enabling high-resolution post processing on host computer
- Support for area and line cameras
- Diverse I/O capabilities: RS422, opto-couplers, LVTTL and 30 V drivers/recievers
- Powerful ecosystem:
  - ✓ Tools for efficient development of both software and FPGA code
  - ✓ Image compression IPs
  - ✓ InfiniVision IP for multi-camera acquisition and synchronization
  - ✓ Supports GenICam's GenTL API and **Halcon™** machine vision software

Target Application Examples

- Automotive and Inspection applications demanding real-time analysis and system response
- Military & Aerospace applications with real-time and post-acquisition analysis
- Medical & Scientific applications requiring high-resolution imaging capabilities
- Traffic & Transportation applications processing high-volume data from multiple locations



The Gidel HawkEye-CXP CoaXPress frame grabbing and real-time image processing system provides the core infrastructure required to realize the most demanding vision and imaging applications.

The HawkEye series offers a number of options to accommodate diverse application needs, from plug-and-play high-performance frame grabbers to a full system solution comprising acquisition, open-FPGA image processing, and flexible custom camera interface. Off-the-shelf HawkEye solutions include support for CoaXPress and Camera Link cameras.

The HawkEye-CXP is CoaXPress Version 1.1 compliant and supports up to four CoaXPress (cXp-6) channels. The HawkEye-CXP family is based on PCIe Gen. 3 x8, providing CPU-free ultra-fast offload capacity of up to 64 Gb/s. Huge data buffers of up to 16 GB fortify the acquisition bandwidth and the image processing capabilities on powerful Arria 10 FPGA.

The board is supported by a comprehensive and powerful ecosystem that includes the Proc Developer's kit, image compression IPs and the InfiniVision IP for multi-camera (up to 100) acquisition and synchronization.

Gidel's Proc Developer's kit is composed of the ProcFG GUI application, an API library, examples, GenICam GenTL API for camera configuration/streaming, and the ProcWizard application for efficient development of image processing algorithms on FPGA.

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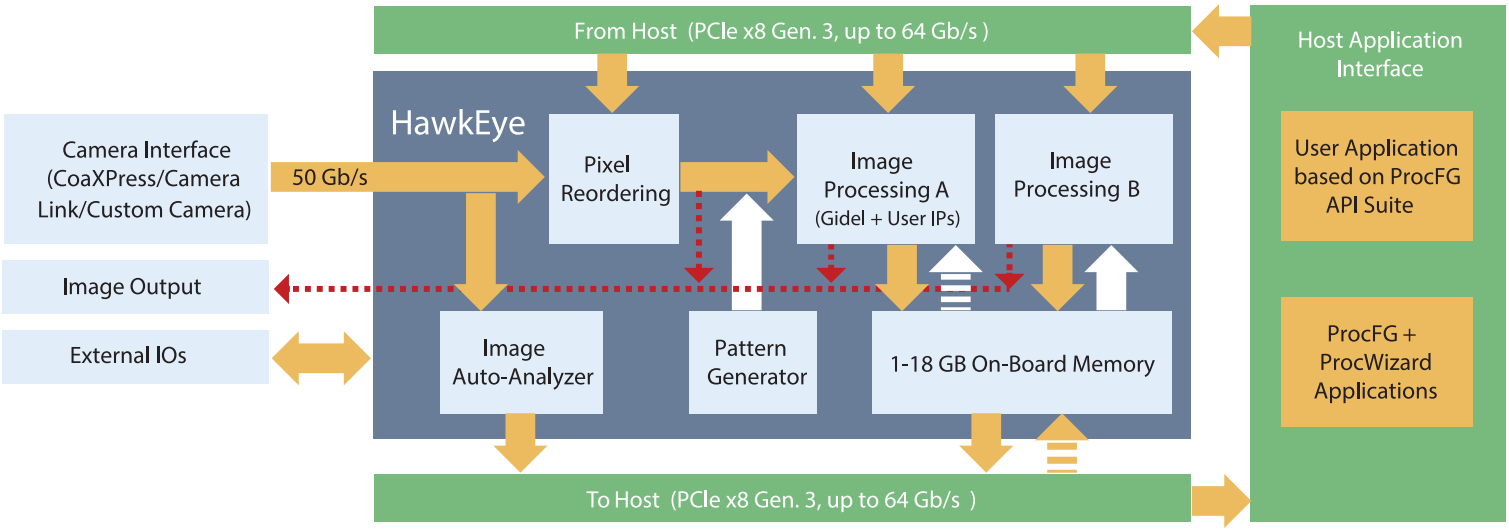
HawkEye-CXP CoaXPress Frame Grabbing and Image Processing System

FEATURE	SPECIFICATIONS
Camera Interface	4x CoaXPress (cXp -6), PoCXP
Image Formats	Mono, Bayer, RGBA (8, 10, 12, 14 and 16 bits/color) and RGB (8, 10 and 12 bits/color).
Max Resolution	Horizontal: 16 K pixels (64-bit) Vertical: 65 K lines
Acquisition Rate	Up to 25 Gb/s acquisition rate
Host Bus	PCIe x8 Gen. 3
Host Throughput	Up to 64 Gb/s
Frame Buffer	1-16 GB
Image Processing	For open FPGA grabber version, option for adding image processing code on Altera Arria 10 FPGA
Camera Types	Area and Line
MTBF	> million hours
Operating Ambient Temperature	0 – 54 C, relative humidity up to 90% (non-condensing)

FEATURE	SPECIFICATIONS
Form Factor	PCIe low-profile
Connectors	• 1, 2, or 4x Mini HD or DIN 1.0/2.3 • VGA15-pin I/O
GPIO	RS422, opto-coupler, LVTTL and 30V at 0.9A
Advanced Features	Selective ROI acquisition
Ecosystem Support	• ProcFG GUI, API and examples. • ProcWizard Developer's tool for efficient FPGA design and software development (for open FPGA version) • Image Compression and Decompression IPs • InfiniVision IP for multi-camera aquisition and synchronization • Supports GenICam GenTL API • Support for MVTec Halcon™ machine vision software



Typical HawkEye acquisition and processing system implementation

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HawkEye-20G

20 Gbps Arria 10 FPGA Computation Accelerators

Key Features

- Altera Arria 10 GX FPGA, 160 or 480
- PCIe x8 Gen. 3 Express or stand-alone
- Form factor: low-profile
- Low-power, starting at less than 12W
- 2 SFP+ cages
- Cost-effective starting at < $1,000
- Dedicated features that enable tailoring to vertical markets
- Up to 1.2 GFLOPS processing capability
- Multi-level memory structure (18+ GB) Sustained throughput of 128+ TB/s for internal memories and ~16 GB/s for on-board memory as follows:
  - Enhanced MLAB (640-bit) SRAM blocks
  - Up to 28,620 M20K (20K-bit) SRAM blocks (572 Mb) at a throughput of up to 128 TB/s at 450 MHz
  - 2 GB DDR4 on-board memory at a maximum sustained throughput of 5.4 GB/s
  - 8-16 GB DDR4 ECC SoDIMM Bank for maximum sustained throughput of 10.8 GB/s (480 device only)
  - On board user flash (optional)
- Typical system freq: 150-450 MHz
- Flexible clocking system
- Supported by Gidel's Developer's Kit
  - Simultaneous acceleration of multiple applications or processes
  - Unmatched HDL design productivity
  - Simple integration with software applications
  - Data compression and data management IPs
- Supported by Gidel's OpenCL BSP and HLS (I++) ASP based on Intel's SDK (for Arria 10 480 only)

The HawkEye is low profile PCIe accelerator based on Altera's (Intel) Arria 10 FPGAs. The platform boasts up to 18 GB DDR4 on-board memory, 2 SFP+ links for a maximum of 28 Gb/s, and a PCIe x8 Gen. 3 host interface. The Arria 10 FPGA provides up to 480K LEs and IEEE floating-point capability. The HawkEye's memory scheme comprises embedded SRAM memory with a throughput capability of up to ~128 TB/s, 1-2 GB DDR4, and up to 16 GB of DDR4 SoDIMM (only for boards with 480 devices). The DDR memory may be accessed via up to 48 parallel ports simultaneously.

The HawkEye accelerator board exhibits an impressive power efficiency, starting at less than 12W. The board is fortified by abundant I/O interface possibilities, including RS422, Opto-coupler, external clock, LVDS, LVTTL (3V), and 30V/0.9A output. The HawkEye can operate as a PCIe-based platform or as a stand-alone compute accelerator. The system has been designed for exceptional high reliability with an MTBF beyond 1 million hours.

The HawkEye is supported by Gidel's unique proprietary tools for developing on FPGA. These tools offer a solution that is unique in the market and can be used together with Intel's design tools to achieve unmatched development efficacy and efficiency. The Gidel development tools suite includes Gidel's Developer's kit, data compression and management IPs, as well as Gidel's OpenCL BSP and HLS (i++) ASP.

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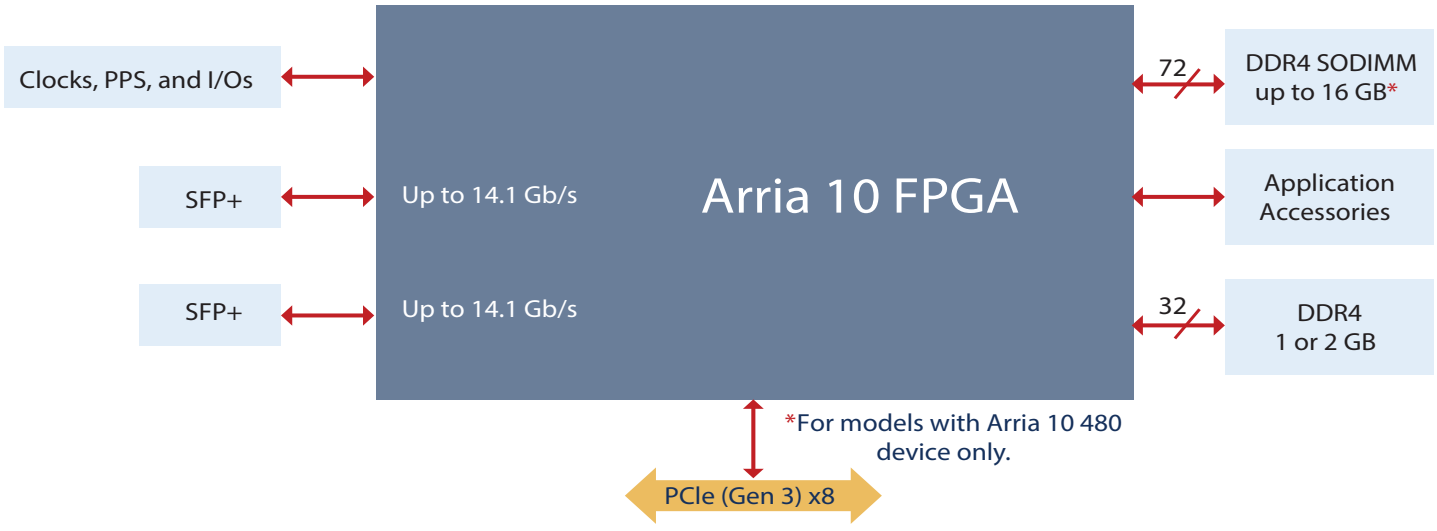
HawkEye - 20 Gbps Arria 10 FPGA Computation Accelerators

FEATURE	SPECIFICATIONS
Form Factor	PCIe low-profile
FPGA	• Intel Arria 10 GX • 160K or 480K Logic Elements • Embedded 18x19 Multipliers • Embedded M20K and MLAB blocks • 2x 12.5/14.1 Gb/s transceivers • 1.6 Gb/s LVDS performance
Memory	• Embedded MLAB (640-bit) SRAM blocks • M20K (20K-bit) SRAM blocks • Up to 16 GB DDR4 SDRAM (SoDIMM) • On board 2GB DDR4 SDRAM
Processing Performance	• Up to 1,431 M20K blocks @ 450 MT/s for total of ~128 TB/s • MLAB blocks@ 450 MT/s • Up to 2 GB DDR4 SDRAM for total of 5.6 GB/s • Up to 16 GB DDR4 SDRAM for a total of 10.8 GB/s • Up to 2,736 18x19 Multipliers

FEATURE	SPECIFICATIONS
Host Interface	PCIe x8 Gen.3
I/O	2x SFP+
GPIO	• RS422 • Opto-coupler • LVDS and LVTTL (3V) • 30V/0.9A output driver • External clock
Development Tools	• Gidel ProDev Kit for HDL design flow: ✓ Generation of dedicated application driver ✓ Splitting of physical on-board memories into logical memories with independent parallel access to/from user logic ✓ Generation of environment FPGA code, including all board/IP constrains and user logic wrapper ✓ Data compression and data management IPs • HLS (i++) ASP and OpenCL BSP • Intel Tools: Quartus+ QSys and DSP builder



HawkEye System Block Diagram

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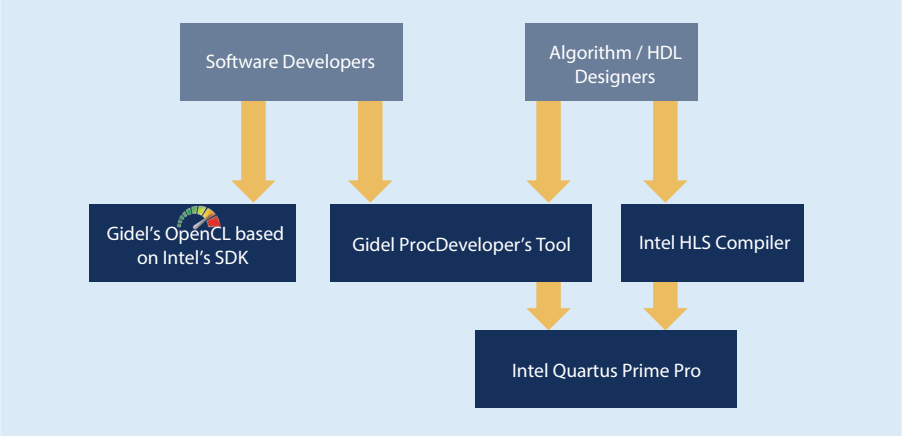
Gidel Developer's Tools

Powerful tools for accelerating development on FPGA

Key Features

- Support for OpenCL based on Intel's SDK, targeting software engineers who want to accelerate applications on FPGA
- HLS Application support package for compiling C++ to HDL, targeting algorithm and HDL designers
- Gidel's Developer's tools for efficient HDL design development:
  - Optimizes system performance
  - Simplifies HDL development tasks and integration with software
  - Automatic generation of HDL envelope and respective software application drivers
  - Generation of PCIe bridge and host interface
  - Debugging tool that directly accesses and controlles the FPGA
  - Ability for multiple programs/ processes to be accelerated concurrently on the same FPGA
  - Memory controller IPs
- Key Benefits of Developer's tools:
  - Dramatically improves project development speed
  - Cuts development cycle time and budget while improving design reliability by enabling on-the-fly debugging
  - Easy maintenance — release a patch within a day
  - No need to spend time on writing documentation
  - Simplifies the interaction between hardware and software developers



Gidel's developer's suite and IPs provide a powerful set of tools and a methodology for simplifying the development task and reducing development time. Gidel's proprietary tools for developing on FPGA offer a market-unique solution that can be used together with Intel's design tools to achieve unmatched development productivity. The Gidel development suite includes the following components:

1. **Gidel's Proc Developer's Kit (ProcDev Kit)** provides an alternative to existing FPGA design methodologies and enables performance to be pushed to the limit. It is easy to use and automatically tailors the process of building the infrastructure required to support algorithm needs by optimizing the use of FPGAs, on-board memory resources, and FPGAs to host communication.

2. **Gidel's HLS Application Support Package (I++)** enables the use of Intel's high-level synthesis (HLS) tool, which takes C++ as input and generates register transfer level (RTL) optimized for FPGA. This tool accelerates the verification time over RTL by orders of magnitude and requires significantly fewer lines of code.

3. **Gidel's OpenCL Board Support Package (BSP)** enables software developers to use the FPGA for accelerating computation. The OpenCL design entry methodology simplifies programming, reducing development time compared with traditional HDL design flow. The bundle provides the means to develop on Gidel's FPGA acceleration boards using C-syntax language.

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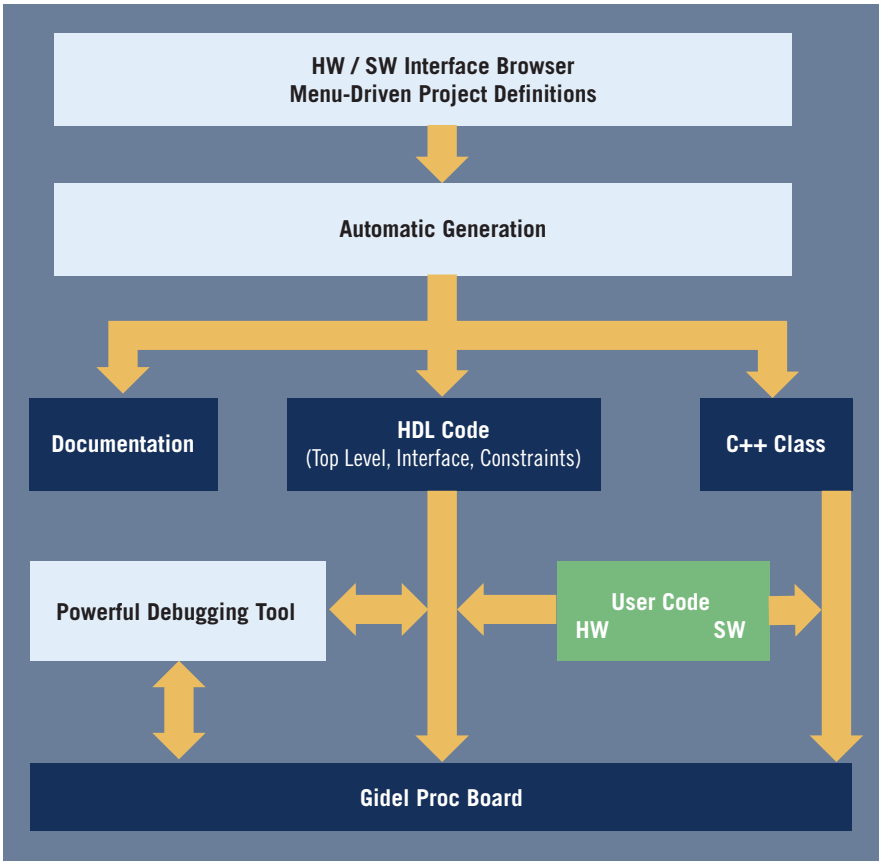

The Gidel ProcWizard Development Flow

- Automatic integration of software and hardware
- HDL code generation (top-level design, PCI interface sub-design, board constraints)
- Automatic integration of Gidel IP cores into the design
- C++ class application driver generation
- Interface documentation generation (HTML or Microsoft Word style)
- Certification of partition generation
- Hardware debugging
- Simple, easy-to-use menu-driven interface
- Automatic hardware initialization and clock setting
- Automatic FPGA loading
- Automatic DMA manipulations

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InfiniVision

Multi-Camera Frame Grabbing and Processing System

Key Features

- Grabbing and synchronizing up to 100 cameras
- Grabbing capability of varying incoming data size
- Option for adding inline Image Signal Processing (ISP)
- Option for inline image compression
- Support for CoaXPress, Camera Link,and MIPI.
- Ability to tailor to any camera interface and protocol
- Acquisition rate of up to 50 Gb/s per board
- Up to 16 GB image frame buffer
- PCIe Gen. 3 host interface at up to 64 Gb/s CPU free host offload capacity
- Diverse I/O capabilities: RS422, opto-couplers, LVTTL and 30 V drivers/recievers
- Powerful image processing capabilities on Intel FPGA devices
- Supported by the Gidel Developer's suite for simplifying and accelerating development on FPGA.
- Support for GenICam GenTL and MVTec's HALCON machine vision software

Target Applications

- Broadcasting and Video
- Augmented Reality
- Video and Audio Compression
- Smart Cities
- Surveillance
- Sorting Machines

The Gidel InfiniVision™ provides flexible infrastructure for acquisition and processing from multi-cameras/sensors simultaneously. The system can capture data streams of varying frame data size as well as to synchronize between up to 100 cameras/sensors. Camera interfaces currently offered by Gidel include CoaXPress, Camera Link, MIPI as well as an option for customization of the camera/sensor interface and protocol. The acquisition path enables adding data processing blocks such as ISP (Image Signal Processing) and compression.

InfiniVision can capture multiple image streams in two ways:

1. From many cameras examining a single scenario.
2. From a single camera capturing images of a single scenario at varying angles.

In both cases, InfiniVision enables building a full coherent image based on multiple synchronized images. The synchronization mechanism automatically re-synchronizes data streams that may have been momentarily interrupted.

InfiniVision's ability to grab on-the-fly any incoming data size adds another dimension of flexibility enabling Imaging applications to combine images of various sizes arriving, for example, from different camera types or from selective ROIs of variable sizes.

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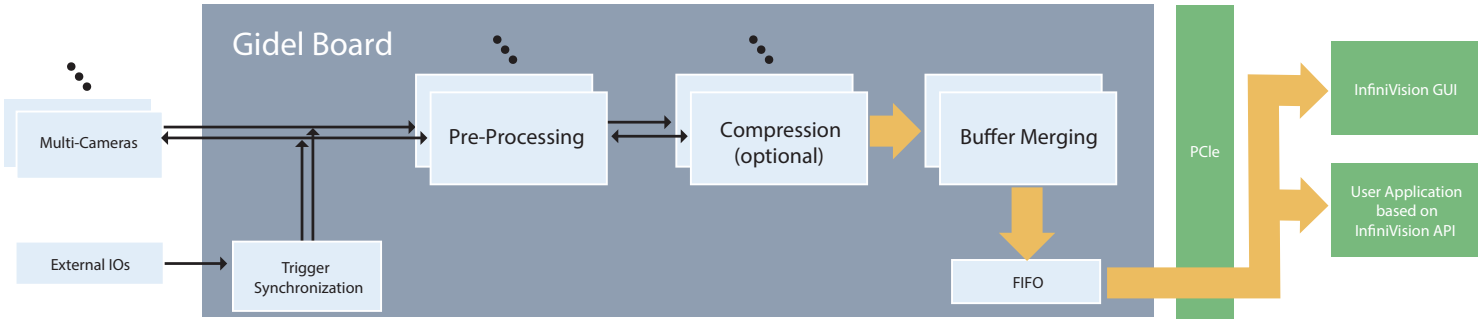
InfiniVision Multi-Camera Frame Grabbing and Processing System

FEATURE	SPECIFICATIONS
Acquisition Rate	Up to 50 Gb/s per board
Cameras Supported	CoaXPress, Camera Link, MIPI6 and option for tailoring to any camera interface/protocol
Pixel Formats Supported	Mono, Bayer, RGBA (8, 10, 12, 14 and 16 bits/color) and RGB (8, 10 and 12 bits/color).
Trigger Synchronization	Up to a 100 cameras
Connectors	SDR26 (for Camera Link) DIN 1.0/2.3 (for CoaXPress) MIPI CSI-2 (for MIPI6) VGA15-pin (for GPIO) Option for custom connector
FPGA	Intel Arria 10
Host Bus	PCIe x8 Gen. 3
Host Throughput	Up to 64 Gb/s
Form Factor	PCIe low-profile

FEATURE	SPECIFICATIONS
GPIO	RS422, opto-coupler, LVTTL and 30V at 0.9A
Software and Ecosystem Support	• API suite and examples. • ProcWizard Development tool for efficient FPGA development • Option for evaluation and simulation using the Gidel CamSim camera simulator • Support for GenICam GenTL and MVTec's Halcon machine vision software
Customization Options	• camera/sensor interface and protocol • Image Signal Processing on FPGA • On-FPGA image compression • Option for Gidel to perform the customization according to user specifications

The Gidel InfiniVision system consists of an FPGA board, firmware, camera interfaces, PCIe interface, GUI Application and API library. The following figure shows a typical system implementation.



InfiniVision System Block Diagram

The InfiniVision acquisition path is from the source cameras to the Gidel Board that pre-processes, compresses (optional) and finally merges the multi-camera image streams into a FIFO buffer. The data is then offloaded via the PCIe interface to an external host application. For simulation or evaluation purposes, the Gidel CamSim can be used to simulate the cameras. The InfiniVision or a User application based on Gidel's API configures and controls the system, implements the host post-processing and displays the grabbed image streams.

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Real-Time JPEG Compression

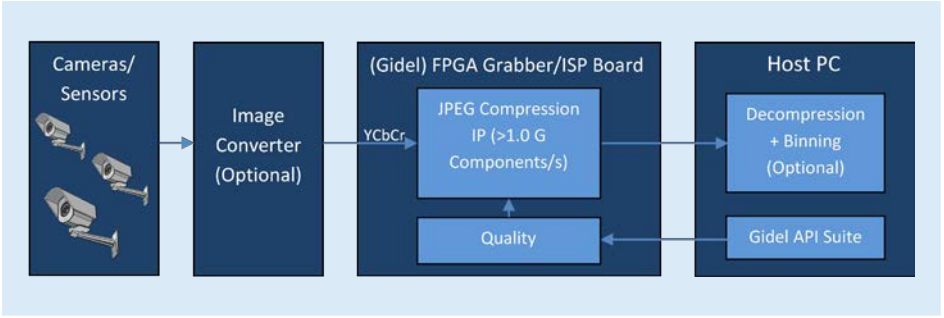
For High-Performance Camera Streams

Key Features

- Real-time JPEG compression of high performance sensor image streams
- IP for FPGA based frame grabbers
- Compression performance beyond 1 Giga components/s
- Architectural design enabling significant performance enhancement
- Support for 422, 444 and 420 color subsampling encoding
- For 422 sampling, throughput beyond 500 MPixels/s
- Ultra-compact IP
- Low latency
- Selectable JPEG compression quality
- Host interface with API suite for software control
- Support for virtually unlimited image width using minimal memory resources
- Supported by Gidel's reconfigurable acquisition flow enabling adding compression and ISP blocks
- Supported by Gidel's InfiniVision IP for acquisition from multi-cameras/sensors
- Supported by the Gidel's Dev Kit for highly efficient development on FPGA
- Optional binning decompression software
- Option for software model for compression simulations

Target Applications

- Recording Systems
- Broadcasting and Video
- Smart Cities and Surveillance
- Autonomous Cars
- Embedded Vision



The Gidel JPEG compression (encoder) IP, gil_jpeg_encode, enables high-performance JPEG compression on FPGA. The compression IP is unique in its fast processing capacity, low latency and compact silicon utilization. As a result of its compactness, the IP can be implemented on a small FPGA device to compress high-performance camera image streams or, alternatively, the IP can be instantiated multiple times on a single larger FPGA device. The IP includes a host interface and an API suite for software control.

The JPEG IP's input stream is in YCbCr format with an optional converter from RGB, monochrome, etc. The degree of compression can be adusted allowing selectable tradeoff between storage size and image quality. Color subsampling can be encoded in 4:2:2, 4:4:4 or 4:2:0 formats. The following table shows a compression performance example using 4:2:2 encoding at 540 MPixels/s. The latency for this example is 130 uS.

FPGA	Throughput	Line size	Bit/ component	Area (ALMs)	M20K	DSP blocks
Arria 10 (slowest device)	1,080 Mega components/s	8K pixels/line	8	5000	151	64

Compression Performance Example

The IP is supported by Gidel's comprehensive ecosystem allowing tailoring optimized solutions that may include image processing, vision algorithms and a concurrent recording system. Recording system may also be complemented by Gidel's CamSim playback system.

The IP is also supported by optional software for image binning decompression. This feature, for example, can be used for displaying videos from multi-cameras during a recording session or for quickly reviewing a large image set.

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Gidel's Supporting Ecosystem

The Gidel ecosystem includes infrastructure and development tools enabling to quickly develop a high-end custom FPGA frame grabber with real-time compression and image processing capabilities. The ecosystem includes:

- ***FPGA Frame Grabber and Image Processing Systems***

Gidel offers FPGA-based systems with open reconfigurable acquisition flow allowing the user to customize the grabbing and to add user image processing blocks including the JPEG compression IP. The frame grabber boards interface with the host computer via PCIe or alternatively may operate as a standalone system.

- ***FPGA Multi-Camera Acquisition System***

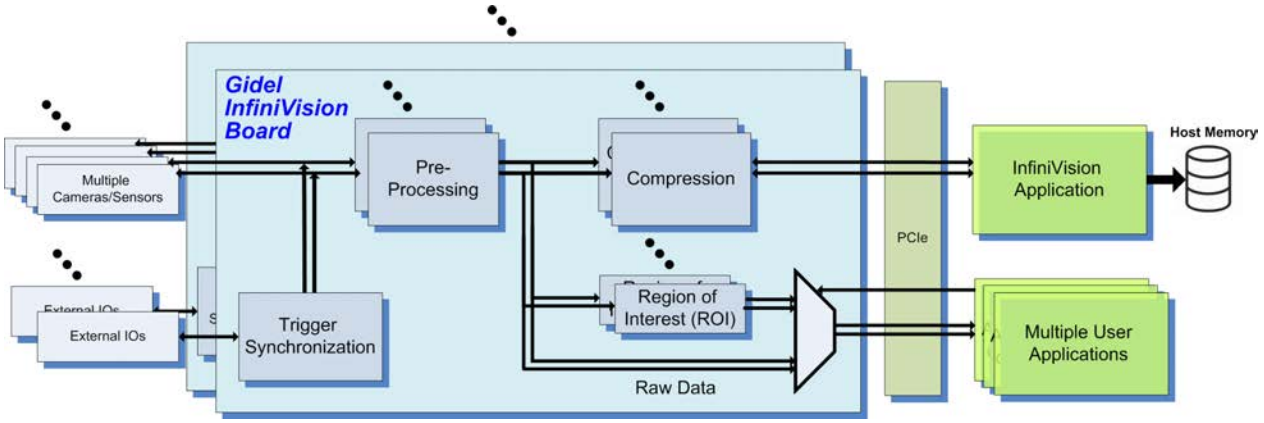
The Gidel InfiniVision is a unique image acquisition system designed for grabbing from multi-cameras/sensors. Combined with real-time compression as much as 100 camera video streams can be supported simultaneously.

- ***Highly Efficient Video Recording & Playback Systems***

Based on real-time compression, Gidel offers a recording system that is exceptionally efficient in both its offloading throughput and compactness of required memory resources. This capability has significant benefits for applications with demanding bandwidth and/or memory resources, e.g., field applications. Based on Gidel's CamSim a playback sub-system, images can then be retrieved at the original throughput for a variety of application tasks.

- ***Proc Developer's Kit***

The Proc Developer's tools enable to map the FPGA board to the desired data flow and interfaces. The following figure demonstrates one possible implementation using InfiniVision, compression and custom image processing.



- ***Gidel Customization Services***

Based on 25 year experience, Gidel offers customization services for developing tailored Vision/Imaging systems according to the customer's specifications. Gidel takes advantage of its uniquely flexible and powerful infrastructure to quickly implement the target application within impressive short time spans.

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Real-time Lossless Compression

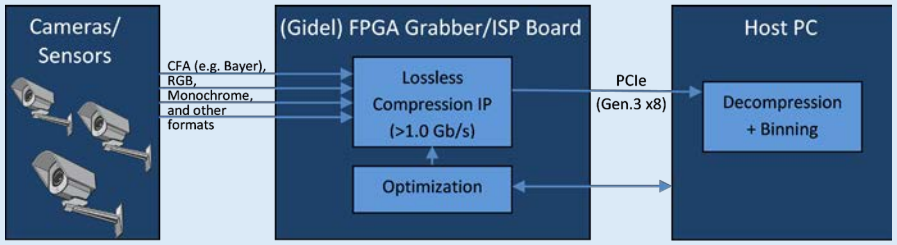
For Bayer, Monochrome, RGB and more

Key Features

- Real-time compression of Color Filter Array (e.g., Bayer), RGB, Monochrome images. For other image formats, contact Gidel.
- Lossless compression
- Compression of camera rates beyond 1 Giga pixel/s
- IP for FPGA based frame grabbers
- Ultra-compact IP (typical< 1000 ALMs)
- Supported by Gidel's reconfigurable acquisition flow enabling adding compression and ISP blocks
- Supported by the Gidel InfiniVision IP for acquisition from multi-cameras/sensors
- Supported by the Gidel Developer's Tools
- Compression optimization based on training using sample data
- Option for on-the-fly optimization using real-time training algorithms
- Option for visually lossless compression fitting for processing quality
- Decompression software with latency of less than one frame period
- Binning option to increase decompression rate by image resize
- Option for software model for compression simulations

Target Applications

- Recording Systems
- Broadcasting and Video
- Smart Cities
- Surveillance
- Autonomous cars



Gidel's lossless compression IP targeting FPGA performs real-time compression for Color Filter Array (CFA - e.g., Bayer), Monochrome and RGB images and videos. The IP enables compression of multi-cameras/sensors at pixel clock rate exceeding 1 Giga pixel/s while using very small FPGA resources and minimal power consumption. The compression is highly efficient and in real-case video applications has achieved a lossless compression ratio of 1:2.3.

FPGA	Throughput	Line size	Bit/pixel	ALM	M20K	DSP blocks
Arria 10 (slowest device)	**540 Mega Pixels/Sec**	**6K**	**8**	**973**	**9**	**9**

Typical example of required FPGA resources

The IP is supported by Gidel's comprehensive eco-system allowing tailoring optimized solutions that may include image processing, Vision algorithms and a concurrent recording system. Recording system may also be complemented by Gidel's CamSim playback system.

There are two compression modes: 1. Compression of individual image frames. 2. Compression of video using I and P frames. The compression can be optimized either by pre-training based on sample images data or by on-the-fly training based on real-time data.

The IP is supported by a decompression software enabling:

- Full streaming rate with a latency of less than a single frame period.
- Binning option to reduce image size and processing time. This feature, for example, can be used for displaying videos from multi cameras during a recording session.

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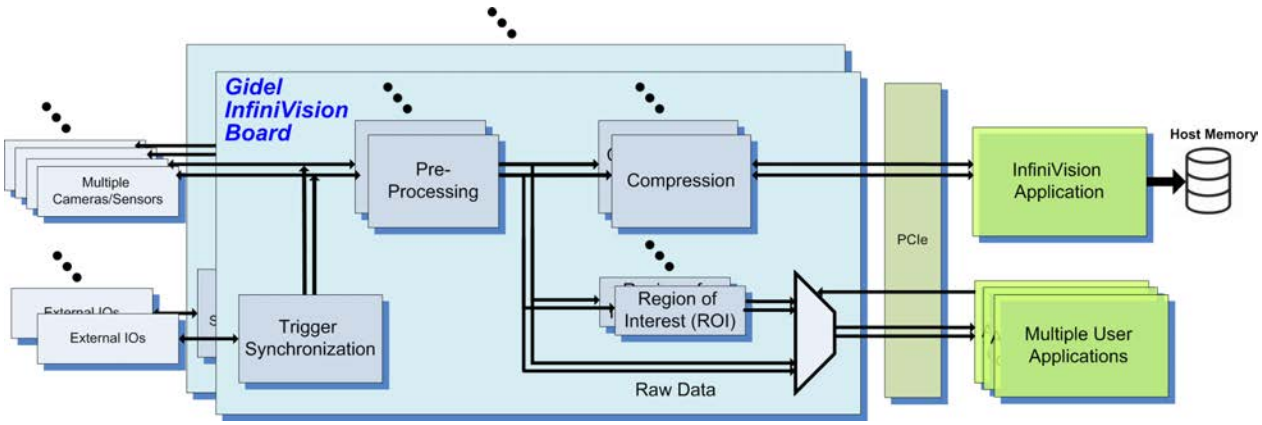

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Proc10A

PCIe x8 (Gen. 3) FPGA Computation Accelerators

Key Features

- Altera Arria 10 FPGA (GX, SX), 1150
- PCIe x8 Gen. 3 or stand-alone
- Up to 15×14.2 Gb/s reconfigurable transceivers supporting multiple protocols and data rates
- Form factor: PCIe half-length
- Up to 40 GFLOPS-per-Watt
- 1x QSFP, 3x QSFP+ and Gidel high-speed connectors
- Multi-level memory structure (18+ GB) Sustained throughput of 128+ TB/s for internal memories and ~16 GB/s for on-board memory as follows:
  - Enhanced MLAB (640-bit) SRAM blocks
  - Up to 2,713 M20K (20K-bit) SRAM blocks (53 Mb) at a typical throughput of 10 TB/s at 450 MHz
  - 1 GB DDR3 on-board memory at a maximum sustained throughput of 5.6 GB/s
  - 2x16 GB DDR4 ECC SoDIMM Banks for maximum sustained throughput of 19.2 GB/s
  - On board user flash (optional)
- Typical system freq: 150-450 MHz
- Flexible clocking system
- Low power (8-70W)
- Supported by Gidel's OpenCL BSP and HLS (I++) ASP based on Intel's SDK
- Supported by Gidel's Developer's Kit
  - Simultaneous acceleration of multiple applications or processes
  - Unmatched HDL design productivity
  - Simple integration with software applications

The Proc10A™ system is a flexible, high-performance, low-power FPGA platform based on Altera's powerful Arria 10 FPGA. The Proc10A's unique architecture balances high performance and flexibility to meet demanding and versatile HPC requirements.

With up to fifteen 14.2 Gb/s full-duplex transceivers and vast memory resources, the Proc10A offers tremendous I/O throughput along with powerful on-board processing and data management capabilities ideal for low latency, high performance HPC, storage, networking, and high-end imaging applications. A multi-level memory scheme includes up to 32 GB DDR3 ECC SODIMM, on-board 1 GB DDR3 SDRAM, dedicated FPGA memory blocks (M20K and MLABs), and other memory options.

In addition, the Proc10A hosts an 8-lane PCI Express Gen. 3 bridge that enables strong co-processing between the host CPU and the FPGA accelerator. For tightly-coupled FPGA and CPU processing, Gidel offers the Proc10A SoC family, with an embedded ARM processor based on the Arria 10 SoC FPGAs.

The Proc10A is supported by OpenCL, HLS, and Gidel's innovative development tools, and enables high productivity based on C and HDL designs.

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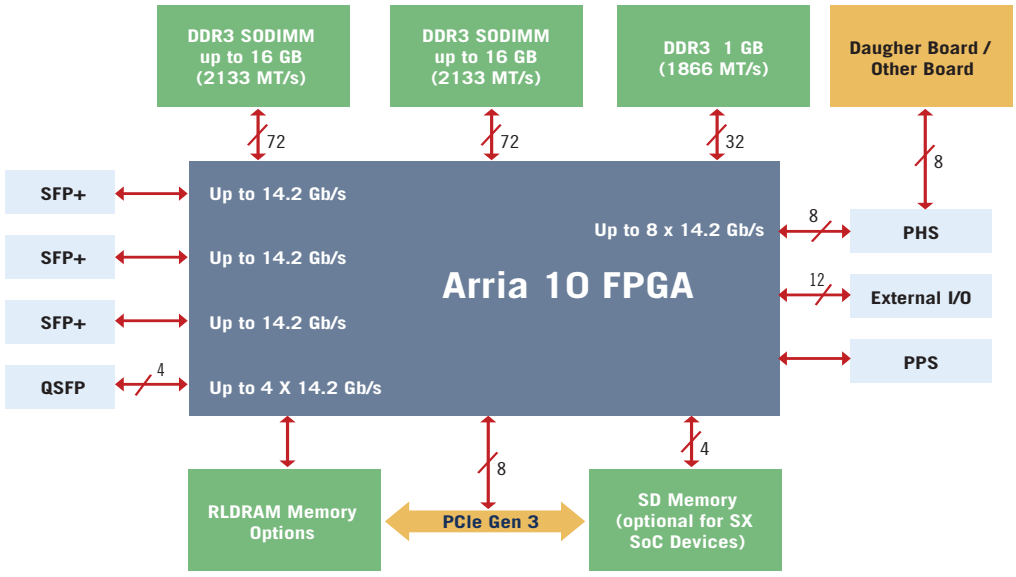
Proc10A - PCIe x8 (Gen. 3) FPGA Computation Accelerators

FEATURE	SPECIFICATIONS
FPGA	• Intel Arria 10 GX • Up to 1150K Logic Elements • Embedded 18x19 Multipliers • Embedded M20K and MLAB blocks • Up to 15x 12.5/14.1 Gb/s transceivers • 1.6 Gb/s LVDS performance
Memory	• Embedded MLAB (640-bit) SRAM blocks • M20K (20K-bit) SRAM blocks • Up to 32GB DDR4 SDRAM (2x SoDIMMs) • On board 2GB DDR4 SDRAM
Processing Performance	• Up to 2,713 M20K blocks @ 450 MT/s for total of ~10 TB/s • MLAB blocks@ 450 MT/s • Up to 1 GB DDR3 SDRAM for total of 5.6 GB/s • Up to 32 GB DDR3 SDRAM for a total of 19.2 GB/s • Up to 3,356 18x19 Variable Precision Multipliers
MTBF	> 1.5 million hours

FEATURE	SPECIFICATIONS
Host Interface	PCIe x8 Gen.3
I/O	1x, 2x, and 4x SFP+
GPIO	12x LVTTL
Board Management	• Flexible clocking system • Temperature monitoring • Internal Voltage monitoring

Development Tools	• OpenCL BSP Based on Intel's SDK
	• HLS ASP for use with Intel's HLS compiler
	• Gidel ProDev Kit for HDL design flow:
	  • Generation of dedicated application driver.
	  • Splitting of physical on-board memories into logical memories with independent parallel access to/from user logic.
	  • Generation of environment FPGA code, including all board/IP constrains and user logic wrapper
	• Intel Tools: Quartus Prime Pro including QSys and DSP builder



Proc10A System Block Diagram

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Proc10S

High Performance Scalable Compute Accelerators

Key Features

- Stratix 10 GX/SX FPGA
- Up to 2800K logic elements
- For SX devices, Quad-core 64-bit ARM Cortex-A53 MPCore processor
- PCIe x16 Gen. 3 or stand-alone
- Up to 16x 28.3 Gb/s reconfigurable transceivers (total of 452 Gb/s)
- Form factor: Full-height, double-width, ¾ Length PCI Express card
- Supports up to 250W (including I/Os)
- I/O Options: 4x QSFP28, 2x SFP28, RGMII and Gidel high-speed connector
- Multi-level memory structure(260+ GB):
  - Enhanced MLAB (640-bit) SRAM
  - Up to 11,721 M20K (20K-bit) SRAM (229 Mb) @ up to 58 TB/s sust. access
  - 4 GB DDR4 SDRAM on-board memory at a maximum sustained throughput of 13.5 GB/s
  - Up to 256 GB DDR4 SDRAM (2x(U/R) DIMM banks) for maximum sustained throughput of 48 GB/s
  - Configuration Flash
  - Serial Flash (SPI)
- Max. fabric clock freq: 1 GHz
- Flexible clocking system with dual ultra-low jitter attenuator @ 100 fsec
- Passive or active cooling
- Supported by Gidel's Developer's Kit
  - Simultaneous acceleration of multiple applications or processes
  - Unmatched HDL design productivity
  - Simple integration with software applications
- Supports variety of Intel development tools

Gidel's latest high-performance scalable compute acceleration system, the Proc10S, pushes data processing power to new heights with peak single precision performance of up to 10 TFLOPS. The Proc10S features an Intel Stratix 10 FPGA with up to 2.8 million logic elements, 260 GB DDR4 memory, and an option for SoC Quad-core 64-bit ARM Cortex-A53 MPCore processor . The Proc10S boasts a 16-lane PCIe Gen. 3 host interface and 28.3 Gb/s and 14.1 Gb/s SERDES I/O transceivers for ultra-fast throughput of up to 452 Gb/s. Abundant I/O connectivity options include: 4x QSFP28 or a combination of 2xQSFP28, 2x SFP28 and RGMII/ Gidel proprietary high-speed connector.

The Proc10S offers designers huge logic resources with incredible flexibility and performance capabilities to meet the most demanding design requirements. The Proc10S can address the design challanges of virtually all end markets including HPC, storage, broadcast, medical, and test & measurement.

The Proc10S is supported by Gidel's unique proprietary tools for developing on FPGA. These tools offer a solution that is unique in the market and can be used together with Intel's design tools to achieve unmatched development efficacy and efficiency. The Gidel development tools suite includes the Gidel ProcWizard for automatic generation and integration of HDL and software code as well as Gidel proprietary IPs, including data-compression-decompression IPs, efficient data management IPs and more.

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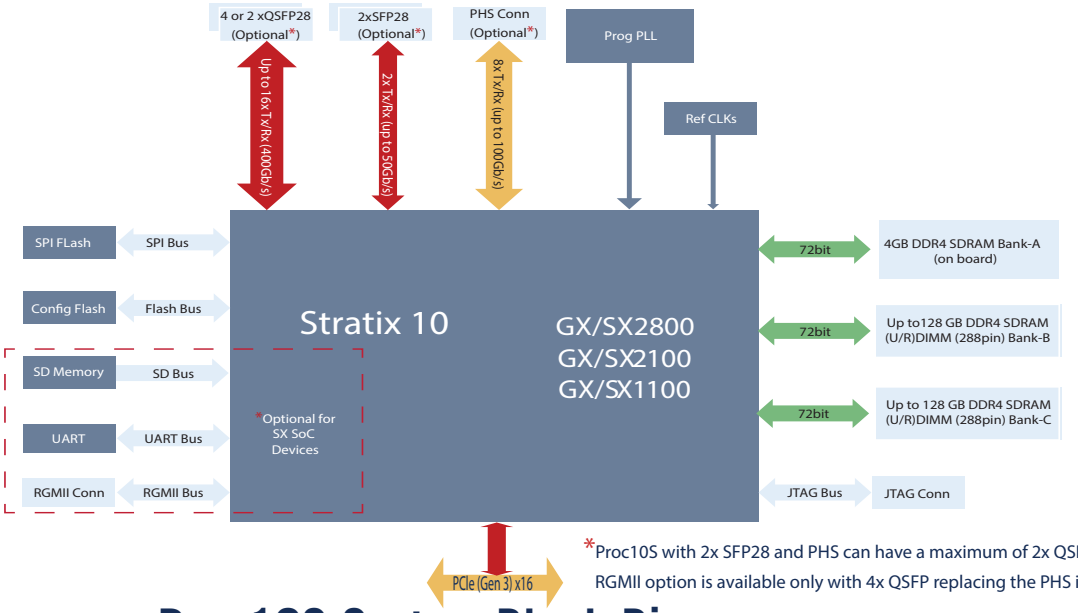
Proc10S - High Performance Scalable Compute Accelerators

FEATURE	SPECIFICATIONS
FPGA	• Intel Stratix 10 GX and SX 2800/2100/1100 • Up to 2800K Logic Elements • H-TILE supporting up to 28.3 Gb/s SERDES I/O • For SX devices, Quad-core 64 bit ARM Cortex-A53 MPCore processor
Memory	• Embedded MLAB (640-bit) SRAM blocks • 11,721 M20K (20K-bit) SRAM blocks • Up to 256 GB DDR4 SDRAM (2x (U/R)DIMMs) • On board 4 GB DDR4 SDRAM
Performance	• Peak fixed-point performance 23.0 TMACS • Peak floating-point performance 9.2 TFLOPS • M20K blocks at up to 58 TB/s sustain access • On board DDR4 SDRAM at up to 13.5 GB/s • (U/R)DIMMs DDR4 SDRAM at up to 48 GB/s • Up to 11,520 18x19 Variable Precision Multipliers • Up to 16x 28.3 Gb/s reconfigurable transceivers • Quad-core 64 bit ARM Cortex-A53 MPCore @ max processor speed of 1.5 GHz • Dual jitter attenuators with accuracy of 100 fs

FEATURE	SPECIFICATIONS
Form Factor	Full-height, double-width, ¾ Length PCI Express
Host Interface	PCIe x16 Gen.3
I/O*	• 4x QSFP28 or 2x QSFP28, 2x SFP28 and Gidel High Speed interface (PHS) • RGMII
Board Management	• Flexible clocking system • Temperature monitoring • Internal Voltage monitoring

Development Tools	• Gidel ProDev Kit for HDL design flow:
	  • Generation of dedicated application driver.
	  • Splitting of physical on-board memories into logical memories with independent parallel access to/from user logic.
	  • Generation of environment FPGA code, including all board/IP constrains and user logic wrapper
	  • Automatic generation and integration of Gidel IPs, including compresssion/decompression IPs, memory controller & data processing IPs, and more
	• Intel Tools: Quartus Pro, QSys and DSP builder



*Proc10S with 2x SFP28 and PHS can have a maximum of 2x QSFP.
RGMII option is available only with 4x QSFP replacing the PHS interface.

Proc10S System Block Diagram

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